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EXAMINER	
VELEZ, ROBERTO	

ART UNIT	PAPER NUMBER
2829	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/595,526	PASTEL, LEAH M. P.	
	Examiner	Art Unit	
	Roberto Velez	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *1-8 and 25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/26/2006,05/16/2006,11/09/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II (claims 9-24) in the reply filed on 0708/2008 is acknowledged.

Claim Objections

2. Claims 10, 13-15 and 21-24 are objected to because of the following informalities: Claim 10 recites "wherein each voltage island". Claim 9, form which claim 10 depends recites "at least one voltage island". For clarity purposes and claim language consistency, Applicant is encouraged to amend claim 10 to recite either "the at least one voltage island" or "each of the at least one voltage island". Claims 13-15 and 21 have similar problem. Claims 22-24 depending from claim 21 are objected for the same reason. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9-11, 13-15, 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennion et al. (US Pat. 5,721,495) in view of Teene (US Pat. 5,726,997).

Regarding claim 9, Jennion et al. shows (Figures 1-6) a method for IDDQ testing, comprising: hot-switching (using 124) at least one voltage island [104] between a global

voltage line (either one of 117, 119 or 121) and a quiescent voltage line [123]; and performing (using 130 and 106) IDDQ testing on the at least one voltage island [104] (as shown in fig. 6).

Jennion et al. fails to disclose wherein the global voltage line and the quiescent voltage line are busses. However, Teene shows (Figures 1-2) a global voltage bus [16] and a quiescent voltage bus [14].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Teene into the device of Jennion et al. by using a global voltage bus and a quiescent voltage bus instead of a global voltage line and a quiescent voltage line. The ordinary artisan would have been motivated to modify Jennion et al. in the manner set forth above for the purpose of being able to simultaneously or alternatively receive and apply different voltage values to verify the operation of the voltage islands.

Regarding claim 10, the combination of Jennion et al. and Teene discloses everything as claimed above in claim 9; in addition, Jennion et al. discloses wherein each voltage island [104] does not lose state during the hot-switching between the quiescent and global voltage busses (Col. 3, Ln 25-39 and specifically Col. 6, Ln 37-39 discloses simultaneously deselecting a power supply and selecting a second power supply in a quiescent state).

Regarding claim 11, the combination of Jennion et al. and Teene discloses everything as claimed above in claim 9; in addition, Jennion et al. discloses supplying a

voltage VDDg [V1, V2 or V3] to the global voltage bus [117, 119 or 121]; and supplying a voltage VDDq [V4] to the quiescent voltage bus [123] (Col. 3, Ln 1-41).

Regarding claim 13, the combination of Jennion et al. and Teene discloses everything as claimed above in claim 9; in addition, Jennion et al. shows (Fig. 1) wherein hot-switching further comprises: providing a connection [116, 118, 120 or 122] between each voltage island [104] and the global and quiescent voltage busses [117, 119, 121 or 123]; and selecting (using 124) at least one of the connections [116, 118, 120 or 122] to connect each voltage island [104] to at least one of the global and quiescent voltage busses [117, 119, 121 or 123].

Regarding claim 14, the combination of Jennion et al. and Teene discloses everything as claimed above in claim 13; in addition, Jennion et al. shows (Fig. 1) wherein each connection [116, 118, 120 or 122] includes a header device [116, 118, 120 or 122], and wherein each connection [116, 118, 120 or 122] is selected (using 124) by activating the header device of the connection via a control signal [124] (Col. 3, Ln 1-65).

Regarding claim 15, the combination of Jennion et al. and Teene discloses everything as claimed above in claim 9; in addition, Jennion et al. discloses wherein performing IDDQ testing comprises: applying a test pattern (voltage from the power supplies) to each voltage island [104], wherein the test pattern remains valid during hot-switching between the global and quiescent voltage busses (Col. 3, Ln 25-39 and specifically Col. 6, Ln 37-39 discloses simultaneously deselecting a power supply and selecting a second power supply in a quiescent state).

Regarding claim 21, Jennion et al. shows (Figures 1-6) a method, comprising: hot-switching (using 124) at least one voltage island [104] between a plurality of different voltage lines (either one of 117, 119, 121 or 123) wherein each voltage island [104] does not lose state during the hot-switching (Col. 3, Ln 25-39 and specifically Col. 6, Ln 37-39 discloses simultaneously deselecting a power supply and selecting a second power supply in a quiescent state).

Jennion et al. fails to disclose wherein the different voltage lines are busses. However, Teene shows (Figures 1-2) different voltage busses [14 and 16].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Teene into the device of Jennion et al. by using different voltage busses instead of different voltage lines. The ordinary artisan would have been motivated to modify Jennion et al. in the manner set forth above for the purpose of being able to simultaneously or alternatively receive and apply different voltage values to verify the operation of the voltage islands.

Regarding claim 24, the combination of Jennion et al. and Teene discloses everything as claimed above in claim 21; in addition, Jennion et al. discloses wherein the voltage busses (either one of 117, 119, 121 or 123) comprise power supply busses or ground busses (Col. 3, Ln 25-39).

5. Claims 12 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennion et al. (US Pat. 5,721,495) and Teene (US Pat. 5,726,997) as applied to claims 11 and 21 above, and further in view Akiki et al. (US Pat. 5,294,883).

Regarding claim 9, the combination of Jennion et al. and Teene discloses everything as claimed above in claim 11.

The combination of Jennion et al. and Teene fails to disclose wherein VDDg is equal to VDDq. However, Akiki et al. shows (Fig. 3) wherein VDDg is equal to VDDq (at step 32 and 34 disclose wherein VTT (VDDq) is equal to VDD).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Akiki et al. into the device of the combination of Jennion et al. and Teene by using same voltages for VDDg and VDDq. The ordinary artisan would have been motivated to modify the combination of Jennion et al. and Teene in the manner set forth above for the purpose of using a single power supply to save cost.

Regarding claim 22, the arguments used for the rejection of claims 11-12 and 21 regarding this feature, also apply.

6. Claims 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennion et al. (US Pat. 5,721,495) and Teene (US Pat. 5,726,997) as applied to claim 9 above, and further in view Sugasawara (US Pat. 6,043,672).

Regarding claim 16, the combination of Jennion et al. and Teene discloses everything as claimed above in claim 9.

The combination of Jennion et al. and Teene fails to disclose hot-switching different sets of voltage islands between the global and quiescent voltage busses. However, Sugasawara discloses hot-switching (using 24 or 25) different sets of voltage

islands [12, 14 or 16] between the global [30] and quiescent voltage busses [26 or 28] (Col. 4, Ln 10-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Sugasawara into the device of the combination of Jennion et al. and Teene by hot-switching different sets of voltage islands between the global and quiescent voltage busses. The ordinary artisan would have been motivated to modify the combination of Jennion et al. and Teene in the manner set forth above for the purpose of testing a plurality of voltage islands either simultaneously or alternatively.

Regarding claim 18, the combination of Jennion et al. and Teene discloses everything as claimed above in claim 9.

The combination of Jennion et al. and Teene fails to disclose wherein IDDQ testing is performed on individual voltage islands or sets of voltage islands. However, Sugasawara shows (Figures 2-3) wherein IDDQ testing is performed on individual voltage islands or sets of voltage islands (Col. 5, Ln 27 through Col. 6, Ln 55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Sugasawara into the device of the combination of Jennion et al. and Teene by performing IDDQ testing on individual voltage islands or sets of voltage islands. The ordinary artisan would have been motivated to modify the combination of Jennion et al. and Teene in the manner set forth above for the purpose of identifying areas of unusual quiescent current consumption.

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jennion et al. (US Pat. 5,721,495) and Teene (US Pat. 5,726,997) as applied to claim 9 above, and further in view Cole, Jr. et al. (US Pat. 6,031,386).

Regarding claim 17, the combination of Jennion et al. and Teene discloses everything as claimed above in claim 9.

The combination of Jennion et al. and Teene fails to disclose locating IDDQ defects using a resistance of the quiescent voltage bus. However, Cole, Jr. et al. discloses locating IDDQ defects using a resistance of a resistive load (Col. 7, Ln 44-55). Even though Cole, Jr. et al. does not specifically disclose a resistance of the quiescent voltage bus, it does teach using the resistance of a device to locate an IDDQ defect.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Cole, Jr. et al. into the device of the combination of Jennion et al. and Teene by locating IDDQ defects using a resistance of the quiescent voltage bus. The ordinary artisan would have been motivated to modify the combination of Jennion et al. and Teene in the manner set forth above for the purpose of accurately monitoring the operation of the voltage island.

8. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennion et al. (US Pat. 5,721,495) and Teene (US Pat. 5,726,997) as applied to claims 9 and 21 above, and further in views of Sugasawara (US Pat. 6,043,672) and Inoshita et al. (US PGPUB 2002/0186035).

Regarding claim 19, the combination of Jennion et al. and Teene discloses everything as claimed above in claim 9.

The combination of Jennion et al. and Teene fails to disclose obtaining IDDQ measurements from individual voltage islands or sets of voltage islands during the IDDQ testing; and comparing the obtained IDDQ measurements to other IDDQ measurements. However, Sugasawara shows (Figures 2-3) obtaining IDDQ measurements from individual voltage islands [12, 14 or 16] or sets of voltage islands during the IDDQ testing (Col. 5, Ln 27 through Col. 6, Ln 55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Sugasawara into the device of the combination of Jennion et al. and Teene by locating IDDQ defects using a resistance of the quiescent voltage bus. The ordinary artisan would have been motivated to modify the combination of Jennion et al. and Teene in the manner set forth above for the purpose of monitoring the operation of the voltage islands.

The combination of Jennion et al., Teene and Sugasawara fails to disclose comparing the obtained IDDQ measurements to other IDDQ measurements. However, Inoshita et al. discloses comparing the obtained IDDQ measurements to other IDDQ measurements (Page 2, Paragraphs 0011 and 0012).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Inoshita et al. into the device of the combination of Jennion et al., Teene and Sugasawara by comparing the obtained IDDQ measurements to other IDDQ measurements. The ordinary artisan would have been motivated to modify the combination of Jennion et al., Teene and Sugasawara in the

manner set forth above for the purpose of accurately monitoring the operation of the voltage islands.

Regarding claim 20, the combination of Jennion et al., Teene, Sugasawara and Inoshita et al. discloses everything as claimed above in claim 19; in addition, Inoshita et al. discloseswherein the obtained IDDQ measurements are compared to IDDQ measurements for similar circuitry, or wherein the obtained IDDQ measurements are compared to an average IDDQ measurement (Page 2, Paragraphs 0011 and 0012).

9. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jennion et al. (US Pat. 5,721,495) and Teene (US Pat. 5,726,997) as applied to claim 21 above, and further in view of Inoshita et al. (US PGPUB 2002/0186035).

Regarding claim 23, the combination of Jennion et al. and Teene discloses everything as claimed above in claim 21.

The combination of Jennion et al. and Teene fails to disclose locating IDDQ defects in the at least one voltage island. However, Inoshita et al. discloses locating IDDQ defects in the at least one voltage island [1] (Page 2, Paragraphs 0011 and 0012).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Inoshita et al. into the device of the combination of Jennion et al. and Teene by locating IDDQ defects in the at least one voltage island. The ordinary artisan would have been motivated to modify the combination of Jennion et al. and Teene in the manner set forth above for the purpose of monitoring the voltage island to verify that proper operation is being done.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is 571-272-8597. The examiner can normally be reached on Monday-Friday 8:00am- 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Roberto Velez/
Examiner, Art Unit 2829
10/08/2008

/Ha T. Nguyen/

Supervisory Patent Examiner, Art Unit 2829